DESIGN NOTES

16mW, Serial/Parallel 14-Bit ADC Samples at 200ksps

Design Note 180

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Introduction

The new LTC®1418 14-bit ADC samples at 200ksps, consuming only 16mW from a single 5V supply. Its pin configurable serial or parallel interface is designed to be versatile, easy to use and adaptable, requiring little or no support circuitry in a wide variety of applications. Some of the key features of this new device include:

- 200ksps Throughput
- Low Power: 16mW
- Parallel and Serial Data Output Modes
- 1.25LSB INL Max and 1LSB DNL Max
- Two Input Ranges: 0V to 4.096V with 5V Supply; ±2.048V with ±5V Supply
- NAP and SLEEP Power Shutdown Modes
- Small Package: 28-Pin SSOP

High Performance Without High Power

As shown in Figure 1, the LTC1418 includes a high performance differential sample-and-hold circuit, an ultra efficient successive approximation ADC, an on-chip reference, and a digital interface that allows easy serial or parallel interface to a microprocessor, FIFO or DSP. The LTC1418's factory calibrated 14-bit performance is achieved without requiring any autocalibration cycles. The result is a 1LSB (max) differential linearity error, no missing codes and 1.25LSB (max) integral linearity error guaranteed over temperature.

For AC applications the dynamic performance of the LTC1418 is exceptional. The low distortion, differential sample-and-hold acquires input signals at frequencies up to 10MHz. At the 100kHz Nyquist frequency, the spurious free dynamic range is typically 95dB. The noise is also low with a signal-to-noise ratio (SNR) of 82dB from DC to well beyond Nyquist and a SINAD of 81.2dB as shown in Figure 2.

The LTC1418's superior AC and DC performance is achieved while dissipating just 16mW at 200kHz and 10mW at sample rates below 50kHz, the lowest power of any 14-bit ADC. Two shutdown modes, NAP and SLEEP, make it possible to cut dissipation further at lower sample rates.

NAP mode reduces dissipation by 80% and SLEEP mode reduces dissipation to 10μW.

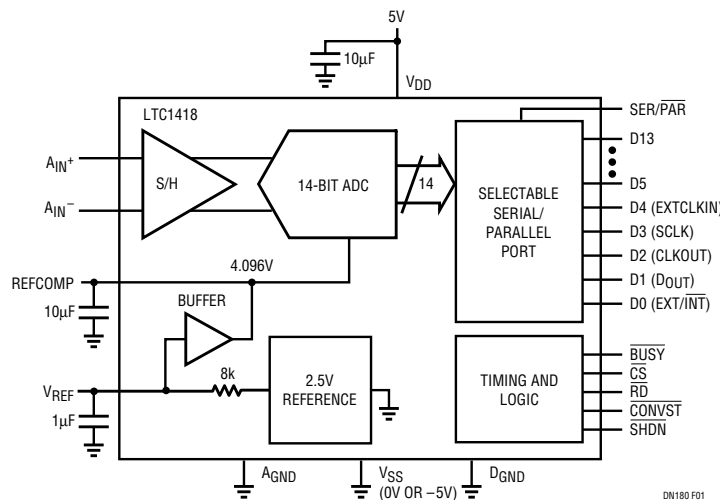*LT, LTC and LT are registered trademarks of Linear Technology Corporation.*

Figure 1. LTC1418 Block Diagram

S/N = 81.2dB
f_{IN} = 97.65625kHz
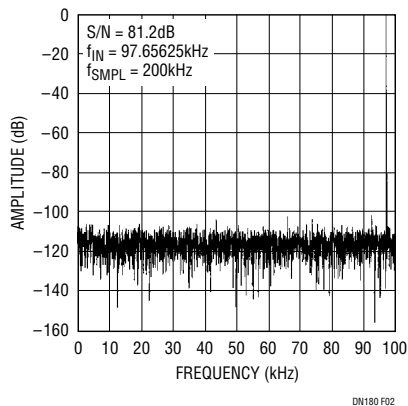f_{SMPL} = 200kHz

Figure 2. LTC1418 FFT

Differential Inputs with Wideband CMRR

The LTC1418's differential input has excellent common mode rejection, eliminating the need for most input conditioning circuitry. As shown in Figure 3, the LTC1418's CMRR remains excellent at high frequencies unlike that of op amps or instrumentation amplifiers whose rejection degrades substantially.
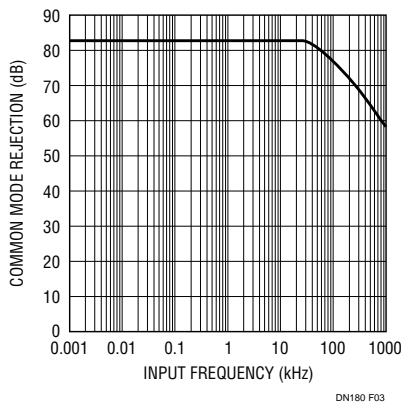

Figure 3. Input Common Mode Rejection vs Input Frequency

Single Supply or Dual Supply Operation

The LTC1418 can operate with single or dual supplies. Dual supplies allow direct coupling of signals that swing below ground. The ADC is equipped with circuitry that automatically detects when –5V is applied to the V_{SS} pin. With a –5V supply the ADC operates in bipolar mode and the full-scale range becomes ±2.048V for $A_{IN}+$ with respect to $A_{IN}–$. With a single supply (V_{SS} = 0V), the ADC operates in unipolar mode with an input range of 0V to 4.096V.

On-Chip Reference

The on-chip 2.5V reference is available on the V_{REF} pin (Pin 3). Internally the reference's 2.5V output is amplified to 4.096V, setting the full-scale span for the ADC. The 4.096V output is available on the REFCOMP pin (Pin 4) and may be used as a reference for other external circuitry. With a temperature coefficient of 10ppm/°C, both V_{REF} and REFCOMP are suitable as the master reference for the system. If, however, an external reference is required, it can easily overdrive either reference output.

Parallel or Serial Data Output

The parallel output mode of the LTC1418 allows the lowest digital overhead. A microcontroller can initiate a conversion and perform other tasks while the conversion is running. The ADC can then signal the microcontroller after the conversion is complete with the BUSY signal, at which time valid data is available on the parallel output bus. BUSY may also be used to clock latches or a FIFO directly since data is guaranteed to be valid with the rising edge of BUSY.

The serial output mode of the LTC1418 is simple and flexible, requiring just three pins for data transfer: a data out pin, a serial clock pin and a control pin. Serial data can be clocked with either the internal shift clock or an external shift clock. Data can be clocked out during or after the conversion. The serial I/O is SPI and MICROWIRE™ compatible.

Perfect for Telecom: Wide Dynamic Range

The wide dynamic range required by telecommunications is satisfied by the LTC1418's low noise, low distortion and extremely wide dynamic range over its entire Nyquist bandwidth. Spurious free dynamic range is typically 95dB to beyond the Nyquist frequency. The sample-and-hold circuit's ultralow, $5ps_{RMS}$ jitter keeps the low SNR constant from DC to 1MHz, ideal for undersampling applications.

The LTC1418 is designed to have ultralow bit error rates, another important requirement for telecom systems. The error rate is so low that it is immeasurable. This, combined with excellent AC and DC specification, makes the LTC1418 ideal for a wide variety of applications.

Conclusions

The new LTC1418 low power, 14-bit ADC will find uses in many types of applications from industrial instrumentation to telephony. The LTC1418's adaptable analog input and digital interface reduces the need for expensive support circuitry and can result in a lower cost, smaller system.

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